IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently Amended) A method of managing power in a graphics controller, which is to be coupled to a processor through a bus, comprising:

receiving a change indication related to a system power supply;

adjusting a first clock, wherein the first clock includes a video clock for a display;

adjusting through a voltage regulator, a graphics controller power supply voltage level in response to the receiving of the change indication related to the system power supply; and

informing by the graphics controller a Video Graphics Array Basic Input /Output System ("VGA BIOS ") with an indication of a change related to the system power supply, wherein the informing includes requesting a set of one or more preprogrammed available clock rates stored in the VGA BIOS;

receiving the set of one or more available clock rates;

checking a state of the graphics controller that includes determining whether a 3D engine or 2D engine is active; and

choosing a desired clock rate from the set of available clock rates based on the checking.

2. (Canceled)

3. (Currently Amended) The method of claim 1 further comprising:

~~receiving the set of one or more available clock rates;~~

~~checking a state of the graphics controller;~~

~~choosing a desired clock rate from the set of available clock rates;~~

adjusting a second clock to conform to the desired clock rate; and wherein:

adjusting the first clock comprises reducing a rate of the first clock; and

adjusting the graphics controller power supply voltage level comprises reducing the graphics controller power supply voltage level.

4. (Previously Presented) The method of claim 3 further comprising:

disabling a CLUT.

5. (Previously Presented) The method of claim 4 wherein:

disabling the CLUT responsive to checking the state of the graphics controller.

6. (Previously Presented) The method of claim 5 further comprising

notifying a system to reduce brightness of a display.

7. (Previously Presented) The method of claim 6 wherein

notifying the system comprises notifying a chipset directly.

8. (Previously Presented) The method of claim 1 wherein

the graphics controller power supply voltage level is associated with a graphics controller power supply internal to the graphics controller.

9. (Previously Presented) The method of claim 1 wherein

the graphics controller power supply voltage level is associated with a graphics controller power supply external to the graphics controller, and adjusting the graphics controller power supply voltage level includes programming the graphics controller power supply with a signal.

10. (Previously Presented) The method of claim 1 wherein

adjusting the first clock comprises increasing a rate of the first clock; and

adjusting the graphics controller power supply voltage level comprises increasing the graphics controller power supply voltage level.

11. (Previously Presented) The method of claim 10 further comprising

increasing a clock rate of the second clock.

12. (Previously Presented) The method of claim 11 further comprising

enabling a CLUT.

13. (Previously Presented) The method of claim 1 further comprising

detecting a change related to a system power supply.

14. (Previously Presented) The method of claim 13 further comprising

installing a software routine in a system containing the graphics controller, the software routine suitable for detecting the change related to the system power supply.

15. (Currently Amended) A method of effecting power management of a graphics controller, which is to be coupled to a processor through a bus, in an operating system comprising:

programming a set of available clock frequencies and storing the set of the available clock frequencies in a Video Graphics Array Basic Input /Output System ("VGA BIOS ");

detecting a change in a system power supply;

notifying the graphics controller of the change;

receiving an indication of power reduction in the graphics controller, wherein the receiving the indication includes receiving a request from the graphics controller for the set of preprogrammed available clock frequencies stored in the VGA BIOS;

providing the set of available clock frequencies to the graphics controller to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether a 3D engine or a 2D engine is active, and

adjusting through a voltage regulator a power supply voltage level supplied to the graphics controller in response to the receiving of the indication the power reduction in the graphics controller.

16. (Previously Presented) The method of claim 15 further comprising

receiving a signal from the graphics controller to reduce brightness of a display.

17. (Previously Presented) The method of claim 16 further comprising

reducing brightness of the display.

18. (Previously Presented) The method of claim 17 further comprising

receiving a software routine suitable for notifying the graphics controller, wherein notifying the graphics controller comprises executing the software routine.

19. (Canceled)

20. (Previously Presented) The method of claim 3 further comprising disabling a first portion of circuitry of the graphics controller.

21. (Previously Presented) The method of claim 20 wherein disabling the first portion of circuitry responsive to checking the state of the graphics controller.

22. (Previously Presented) The method of claim 21 further comprising enabling the first portion of circuitry of the graphics controller.

23. (Currently Amended) A graphics controller, which is to be coupled to a processor through a bus, comprising:

a power supply input configured to receive power at a range of voltages from a voltage regulator;

a power supply control output to provide a trigger signal to the voltage regulator to change a voltage level supplied to the graphics controller through the power supply input when a change indication related to a system power supply is detected;

a first clock output that provides an adjustable video clock for a display, and

a system power supply change input coupled to the first clock output and to the power supply control output to detect the change indication related to the system power supply; and

a system interface coupled to the system power supply change input;

a 2D engine;

a 3D engine;

a control unit coupled to the system interface, the 2D engine, and the 3D engine, wherein the control unit is configured to inform a Video Graphics Array Basic Input /Output System ("VGA BIOS ") through the system interface about the change indication related to the system power supply, wherein the informing includes requesting a set of one or more preprogrammed available clock rates stored in the VGA BIOS, wherein the control unit is to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether the 3D engine or the 2D engine is active.

24. (Previously Presented) The graphics controller of claim 23 further comprising a first clock control output.

25. (Previously Presented) The graphics controller of claim 24 further comprising a memory coupled to the first clock output.

26. (Previously Presented) The graphics controller of claim 24 further comprising a second clock output; and
a second clock control output.

27. (Previously Presented) The graphics controller of claim 26 further comprising a memory coupled to the first clock output.

28. (Previously Presented) The graphics controller of claim 27 wherein:
the memory is integrated with other portions of the graphics controller on a single substrate.

29. (Previously Presented) The graphics controller of claim 27, wherein

the voltage regulator is coupled to the power supply input and the power supply control output to provide the voltage to the graphics controller based on the trigger signal from the graphics controller.

30. (Previously Presented) The graphics controller of claim 29 wherein

the voltage regulator is integrated with other portions of the graphics controller on a single substrate.

31. (Previously Presented) The graphics controller of claim 30 further comprising

a VGA BIOS.

32. (Previously Presented) The graphics controller of claim 26 further comprising

a brightness output configured to signal to a system that a reduction in brightness of a display is appropriate.

33. (Previously Presented) The graphics controller of claim 32 wherein

the brightness output is suitable for coupling directly to a video control chipset.

34. (Currently Amended) The graphics controller of claim 32 further comprising

~~a 2D engine;~~

~~a 3D engine;~~

a CLUT coupled to the 3D engine and coupled to the 2D engine;

a system interface including the system power supply input;

a video interface including the second clock output and the second clock control output;

a power control interface including the power supply input and the power supply control output;

a memory control interface including the first clock output; and

[[a]] wherein the control unit is coupled to the system interface, the CLUT, the video interface, the power control interface, the memory control interface, the 2D engine and the 3D engine.

35. (Currently Amended) A graphics controller, which is to be coupled to a processor through a bus, comprising:

a power supply input configured to receive power at a range of voltage levels from a power regulator;

a power supply control output to provide a trigger signal to the power regulator to change a voltage level supplied to the graphics controller when a change indication related to a system power supply is detected;

a first clock output that provides an adjustable video clock for a display;

a system power supply change input;

a first clock control output;

a second clock output;

a second clock control output;

a brightness output configured to signal to a system that a reduction in brightness of a display is appropriate;

a 2D engine;

a 3D engine;

a CLUT coupled to the 3D engine and coupled to the 2D engine;

a system interface including the system power supply input;

a control unit, ~~wherein~~ coupled to the system interface that is configured to inform a Video Graphics Array Basic Input /Output System ("VGA BIOS") about the change indication related to the system power supply, wherein the informing includes requesting a set of one or more preprogrammed available clock rates stored in the VGA BIOS, wherein the control unit is to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether the 3D engine or the 2D engine is active;

a video interface including the second clock output and the second clock control output;

a power control interface including the power supply input and the power supply control output;

a memory control interface including the first clock output; and

[[a]] wherein the control unit is coupled to the system interface, the CLUT, the video interface, the power control interface, the memory control interface, the 2D engine and the 3D engine.

36. (Currently Amended) A method of managing power in a graphics controller, which is to be coupled to a processor through a bus, comprising

receiving a change indication related to a system power supply;

reducing a rate of a first clock, wherein the first clock includes a video clock for a display;

reducing a graphics controller power supply voltage level through a voltage regulator after the change indication is received;

signaling a BIOS with ~~an indication of a~~ the change indication related to the system power supply by the graphics controller, wherein the signaling the BIOS includes requesting for a set of one or more available clock rates stored in the BIOS, wherein the control unit is to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether a 3D engine or a 2D engine is active;

receiving a set of one or more available clock rates;

checking a state of the graphics controller;

choosing a desired clock rate from the set of available clock rates;

adjusting a second clock to conform to the desired clock rate;

disabling a first portion of circuitry responsive to checking the state of the graphics controller.

37. (New) The graphics controller of claim 23, wherein the graphics controller is coupled to send data to and receive data from a frame buffer.

38. (New) The graphics controller of claim 35, wherein the graphics controller is coupled to send data to and receive data from a frame buffer.